CLAIMS

What is claimed is:

1. A method for synchronizing a clock system comprised of a master time keeper and at least one secondary clock, the secondary clock including a control device in operable communication with the master time keeper, and a time display for exhibiting a time of day, the time display being operable by the control device, comprising the steps of:

sending a correction signal from the master time keeper to the control device of the secondary clock, the correction signal carrying information formatted in one of a plurality of predetermined correction schemes;

receiving the correction signal at the control device; and

automatically analyzing the correction signal received by the control device to determine which correction scheme from the plurality of predetermined correction schemes was used to format the information being carried by the correction signal.

2. The method of claim 1 further comprising the steps of:

determining a time value from the information being carried by the correction signal; and

operating the time display of the secondary clock so as to cause a time of day exhibited on the time display to correspond with the time value determined from the correction signal.

3. The method of claim 2 further comprising the step of storing an initial time exhibited on the time display in a memory location associated with the control device.

4. The method of claim 2, wherein the clock system further comprises one or more position sensors for detecting a position of the display device, the position sensors operably communicating with the control device, and further

comprising the step of determining an initial position of the time display using the position sensors.

5. The method of claim 2, wherein the correction scheme defines the correction signal as an incremental movement.

6. The method of claim 1, wherein the secondary clock maintains real time.

7. A method for synchronizing a clock system comprised of a master time keeper and at least one secondary clock, the secondary clock including a control device in operable communication with the master time keeper, a time display for exhibiting a time of day, the time display being operable by the control assembly, and one or more position sensors for detecting a position of the display device, the position sensors operably communicating with the control device, comprising the steps of:

sending a correction signal from the master time keeper to the control device of the secondary clock, the correction signal carrying information formatted in one of a plurality of predetermined correction schemes; and

sending an encoded signal to the control device for determining which correction scheme from the plurality of predetermined correction schemes to enable on the control device.

8. The method of claim 7, wherein the encoded signal is sent from the master time keeper.

9. The method of claim 7, wherein the encoded signal is sent from a temporary transmitter.

10. The method of claim 9, wherein the temporary transmitter is a wireless transmitter.

11. The method of claim 7 further comprising the step of using the encoded signal to disable a correction scheme.

12. The method of claim 7, wherein the state of the correction scheme is one of enabled or disabled, the state of the correction scheme being stored in a non-volatile memory associated with the control device of the secondary clock.

13. The method of claim 7 further comprising the steps of:

determining a time value from the information being carried by the correction signal based on the determined correction scheme; and

operating the time display of the secondary clock so as to cause a time of day exhibited on the time display to correspond with the time value determined from the correction signal.

14. The method of claim 13 further comprising the step of storing an initial time exhibited on the time display in a memory location associated with the control device.

15. The method of claim 13 further comprising the step of determining an initial position of the time display using the position sensors.

16. The method of claim 13, wherein the correction scheme defines the correction signal as an incremental movement.

17. The method of claim 7, wherein the secondary clock maintains real time.

18. A method for synchronizing a clock system comprised of a master time keeper and at least one secondary clock, the secondary clock including a control device in operable communication with the master time keeper, a time display for exhibiting a time of day, the time display being operable by the control assembly,

and one or more position sensors for detecting a position of the display device, the position sensors operably communicating with the control device, comprising the steps of:

sending a correction signal formatted in an unrecognized correction scheme from the master time keeper to the control device of the secondary clock; and

sending an encoded signal to the control device defining the unrecognized correction scheme.

19. The method of claim 18, wherein the step of defining the unrecognized correction scheme comprises associating a time of day with a corresponding correction signal.

20. The method of claim 18, wherein the step of defining the unrecognized correction scheme comprises associating a time that reoccurs multiple times a day to a corresponding correction signal.

21. The method of claim 20, wherein the multiple reoccurring time occurs twice daily.

22. The method of claim 20, wherein the multiple reoccurring time occurs every hour.

23. The method of claim 20, wherein the multiple reoccurring time occurs every minute.

24. The method of claim 20, wherein the multiple reoccurring time occurs every second.

25. The method of claim 18, wherein the unrecognized correction scheme defines an incremental movement upon receipt of a correction signal.

26. The method of claim 18, wherein multiple encoded signals can be used to define multiple correction signals.

27. The method of claim 18, wherein the encoded signal is sent from the master time keeper.

28. The method of claim 18, wherein the encoded signal is sent from a temporary transmitter.

29. The method of claim 28, wherein the temporary transmitter is a wireless transmitter.

30. The method of claim 18, wherein the secondary clock maintains real time.

31. The method of claim 18 further comprising the steps of:

determining a time value from the information being carried by the correction signal based on the defined correction scheme; and

operating the time display of the secondary clock so as to cause a time of day exhibited on the time display to correspond with the time value determined from the correction signal.

32. The method of claim 31 further comprising the step of storing an initial time exhibited on the time display in a memory location associated with the control device.

33. The method of claim 31 further comprising the step of determining an initial position of the time display using the position sensors.

34. The method of claim 31, wherein the correction scheme defines the correction signal as an incremental movement.

35. A secondary clock for use in a clock system having a master time keeper for transmitting a control signal carrying time information formatted in one of a plurality of predetermined correction schemes, the secondary clock comprising:

a control device configured to receive the correction signal transmitted from the master time keeper, the control device comprising a processor operable for automatically interpreting the correction signal to determine which of the plurality of predetermined correction schemes the master time keeper used to format the control signal; and

a time display for exhibiting a time of day, the time display being operable by the control device in response to the control signal transmitted by the master time keeper.

36. The secondary clock of claim 35, wherein the control device further comprises a non-volatile memory operably connected to the processor for storing data transmitted from the processor to the non-volatile memory.

37. The secondary clock of claim 35 further comprising a motor device operable for changing the time of day exhibited on the time display, wherein the control device further comprises a motor driver interface in communication with the processor and the motor device, the motor driver interface operable for controlling the motor device in response to a signal received by the motor driver interface from the processor.

38. The secondary clock of claim 35 further comprising a positional sensor in communication with the processor, the positional sensor operable for detecting the time of day exhibited on the time display and transmitting a signal to the processor representing the detected time.

39. The secondary clock of claim 35 further comprising a manual switch input for manually transmitting information to the processor.

40. The secondary clock of claim 39, wherein the manual switch input is operable between a first state, wherein a correction scheme is enabled, and a second state, wherein the correction scheme is disabled.

41. The secondary clock of claim 39, wherein the manual switch is operable for inputting a correction scheme into the processor.

42. The secondary clock of claim 35, wherein the control device further comprises:

a power and communication translator and filter configured to receive and condition the correction signal transmitted from the master time keeper; and

a local device power source operably connected to the power and communication translator and filter and the processor, wherein the power and communication translator and filter transmits a control signal to the local device power source in response to the correction signal received from the master time keeper and the local device power source adjusts a voltage of the control signal to a predetermined level prior to transmitting the control to the processor.

43. The secondary clock of claim 35, wherein the control device further comprises:

a power and communication translator and filter configured to receive an electrical pulse transmitted from the master time keeper; and

a communication interrogation circuit operably connected to the power and communication translator and filter and the processor, wherein the power and communication translator and filter transmits a signal to the communication interrogation circuit in response to the electrical pulse received from the master time keeper and the communication interrogation circuit transmits a notification signal to the processor signaling that power and communication translator and filter has received the electrical pulse from the master time keeper.

44. The secondary clock of claim 35, wherein the control device further comprises:

a reset/correction translator and filter configured to receive the correction signal transmitted by the master time keeper, the reset/correction translator and filter operable for determining the polarity of the correction signal;

a communication interrogation circuit operably connected to the reset/correction translator and the processor, wherein the reset/correction translator transmits a signal to the communication interrogation circuit identifying the polarity of the correction signal in response to the correction signal received from the master time keeper.

45. The secondary clock of claim 35, wherein the time display comprises a digital display for exhibiting the time of day as a series of numerical numbers.

46. The secondary clock of claim 35, wherein the time display comprises an analog display having a minute hand and an hour hand for exhibiting the time of day.

47. The secondary clock of claim 35, wherein the control device is configured for receiving an encoded signal for use by the processor in determining which of the plurality of predetermined correction schemes the master time keeper used to format the control signal.

48. The secondary clock of claim 35, wherein the control device is configured to receive an encoded signal from the master time keeper, the encoded signal carrying information defining the correction scheme used by the master time keeper to format the control signal, wherein the encoded signal is usable by the processor for interpreting the time information being carried by the correction signal transmitted from the master timekeeper.

49. A clock system comprising:

a master timekeeper configured to transmit a correction signal carrying time information formatted in one of a plurality of predetermined correction schemes;

at least one secondary clock operably connected to the master time keeper, the secondary clock comprising a control device configured to receive the correction signal transmitted from the master time keeper, the control device automatically operating to determine the correction scheme used to format the time information and to decipher the time information carried by the correction signal based on the determined correction scheme, and a time display for exhibiting a time of day, the time display being controllable by the control device based on the deciphered time information.

50. The clock system of claim 49, wherein each of the at least one secondary clocks are connected in series to the master time keeper.

51. The clock system of claim 49, wherein at least one of the at least one secondary clocks has a digital display for exhibiting the time of day as a series of numerical numbers.

52. The clock system of claim 49, wherein at least one of the at least one secondary clocks includes an analog display having a minute hand and an hour hand for exhibiting the time of day.

53. The clock system of claim 49 further comprising a temporary transmitter for transmitting a control signal to the secondary clock instructing the control device to disable one or more predetermined correction scheme protocols.

54. The clock system of claim 49 further comprising a temporary transmitter for transmitting a control signal to the secondary clock for instructing the control device to enable one or more predetermined correction scheme protocols.